ABSTRACT OF THE INVENTION

According to the present invention, there is provided a semiconductor memory having a memory cell array region and peripheral circuit region, comprising, a gate electrode formed on a semiconductor substrate via a first insulating film in each of said memory cell array region and peripheral circuit region, and including a conductive layer which at least partially includes a silicon layer, and a second insulating film, a first oxide film formed on side surfaces of said conductive layer included in said gate electrode and on said semiconductor substrate in said memory cell array region, a second oxide film formed on side surfaces of said conductive layer included in said gate electrode and on said semiconductor substrate in said peripheral circuit region, and having a film thickness smaller than that of said first oxide film, a first nitride film formed on side surfaces of said gate electrode in said memory cell array region, and a second nitride film formed on side surfaces of said gate electrode in said peripheral circuit region, and having a film thickness larger than that of said first nitride film.